Computer Mathematics

Week 9 Examples

1. Logic gates have a propagation delay, which is the time taken for the output to change to the correct value after one or more of the inputs has changed. If we call the propagation delay through a gate t_p, what is the propagation delay (expressed in terms of t_p) for:

a) the sum output of a full adder? _____ t_p

b) the carry output of a full adder? _____ t_p

c) the output of a 2-way multiplexer? _____ t_p

d) the output of a N-way multiplexer? _____ t_p

2. Consider a 4-bit adder, constructed from four full adders 'daisy chained' together. What is the propagation delay for:

a) the carry out of the most significant bit? _____ t_p

b

b) the four-bit sum? _____ t_p

3. Design a four-way multiplexer. Two select inputs (SEL_1 and SEL_0) control which one of four data inputs (A, B, C and D) are routed to the output (O). Use any technique you like to design the circuit.